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DICKSTEIN SHAPIRO LLP
1825 EYE STREET, NW
WASHINGTON, DC 20006

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/648,311	KAGINELE, SATHYA P.	
	Examiner	Art Unit	
	Christine T. Tu	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12-14,17,19-23,33-35 and 39-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10, 12-14, 17, 19-23, 33-35 and 39-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 112

2. Claims 40-41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 40-41 (depend on claim 36):

Claims 40-41 are rejected because both claims 40 and 41 are depending on a cancelled claim –claim 36.

Claim Rejections - 35 USC § 103

3. Claims 1-10, 12-14, 17, 19-23, 33-35, and 39-42 are again rejected under 35 U.S.C. 103(a) as being unpatentable over Ichiriu (7,002,823) in view of Nataraj et al. (6,944,039 and Nataraj hereinafter).

Claims 1-2:

Ichiriu discloses the invention substantially as claimed. Ichiriu shows (figures 1 & 5) that, in a CAM device (100), a CAM array (101) includes a plurality of CAM cells arranged in rows for storing CAM words. Each CAM cell (201) includes a compare circuit to compare the content of the memory cell with a comparand signal. A comparand register (115) is used to store a comparand value received via the

comparand bus (143) and outputs the comparand value to the CAM array (101). During a compare operation, the comparand may be masked by a global mask value, and then compared simultaneously with all the CAM words stored in the CAM array. Each of the rows of CAM cell is coupled to a corresponding match line (182) and any match between the comparand and a valid CAM word results in a match signal being output to the flag circuit (112). The flag circuit (112) then outputs a match flag signal to indicate that a match has occurred (figures 1 and 5, column 3 line 29 - column 4 line 34, column 6 lines 42-47).

Ichiriu states that a decoder (103) inside the CAM device (100) decodes a selected address to activate one of a plurality of word lines (181) (column 5 lines 17-23, column 3 lines 54-56).

Ichiriu also states at the start of a comparison operation, a feature of precharging each of the match lines (182) to a high logical level (column 6 line 61-column 7 line 4).

Ichiriu further states that, during a compare operation, a respectively portion of the comparand is applied to each column of CAM cells (201) via lines CL/CLB such that the complete comparand is applied to each row of the CAM cells (201) simultaneously. In one embodiment, each of the match lines (182) is precharged to a high logical level at the start of a comparison operation, but pulled down to a low logical level by the compare circuit with any attached CAM cell (201) that receives comparand signals which do not match the stored data value. In this configuration, any match line (182) NOT pull low constitutes a match signal (figure 5, column 6 line 61-column 7 line 4).

Ichiriu does not explicitly teach the feature of confirming proper operation of a control line used to enable output from a match line under test and the feature of enabling output from the match line under test.

Nataraj, however, teaches (figure 4) that a match latch circuit (203), which is connected to precharge circuits (233) and match lines (241), comprises latching circuits (221), each latching circuit comprises an AND gate (223) and a latch element (225). Each AND gate (223) has a first input coupled to receive a detect signal (224) and a second input coupled to a corresponding one of the match lines (241). The AND logic gate (223) outputs a logic-level match signal in high or low state according to whether the signal level of the corresponding match line is above or below a threshold. The latch signal (226) is supplied to a latch enable input of the latch element (225) enables the logic-level match signal to pass through the latch element (225) (figure 4, column 5 lines 30-32 and column 6 lines 48-62).

It would have been obvious to one skilled in the art at the time the invention was made to use Nataraj's match latch circuit (203) having the plurality of AND gates (223) and plurality of latch elements (225) such that each latch element (225) is enabled to pass/output a match signal [generated by a AND gate (223)] to Ichiriu's priority encoder (114) and Ichiriu's FLAG circuit (112). One having ordinary skill in the art would be motivated to combine the teachings of Ichiriu and Nataraj because the combination of Ichiriu's priority encoder [114] & FLAG circuit [112] and Nataraj's priority encoder/flag logic circuit (215) comprises inputs of match signals and outputs of match addresses

and match flag (Ichiriu: figure 1, column 3 line 64-column 4 line 13; Nataraj: figure 4, column 7 line 1-15).

Claim 3:

Ichiriu teaches that the CAM array (101) includes circuitry to force validity value with each validity storage cell (202) to a reset state to prevent assertion of a match signal by pulling the match line low for the corresponding row of CAM cells (column 7 lines 49-65, column 8 lines 20-24).

Claims 4-5:

Ichiriu's decoder (105) is a state machine that transitions from state to state in response to transitions of a clock signal (CLK) (104) (column 4 lines 57-67).

Claims 6-7:

Ichiriu teaches that each row of CAM cells (201) is coupled to a respective match line (182) (figure 5, column 6 lines 33-37).

Claims 8-9:

Ichiriu discloses the invention substantially as claimed. Ichiriu shows (figure 1) that a CAM array (101) includes a plurality of CAM cell arranged in rows for storing CAM words. Each CAM cell (201) includes a compare circuit to compare the content of the memory cell with a comparand signal. A comparand register (115) is used to store

a comparand value received via the comparand bus (143) and outputs the comparand value to the CAM array (101). During a compare operation, the comparand may be masked by a global mask value, and then compared simultaneously with all the CAM words stored in the CAM array. Each of the rows of CAM cell is coupled to a corresponding match line (182) and any match between the comparand and a valid CAM word results in a match signal being output to the flag circuit (112). The flag circuit (112) then outputs a match flag signal to indicate that a match has occurred (figure 1, column 3 line 29 - column 4 line 34, column 6 lines 42-47).

Ichiriu does not explicitly teach the feature of confirming proper operation of a control line used to enable output from a match line under test and the feature of enabling output from the match line under test.

Nataraj, however, teaches (figure 4) that a match latch circuit (203), which is connected to precharge circuits (233) and match lines (241), comprises latching circuits (221), each latching circuit comprises an AND gate (223) and a latch element (225). Each AND gate (223) has a first input coupled to receive a detect signal (224) and a second input coupled to a corresponding one of the match lines (241). The AND logic gate (223) outputs a logic-level match signal in high or low state according to whether the signal level of the corresponding match line is above or below a threshold. The latch signal (226) is supplied to a latch enable input of the latch element (225) enables the logic-level match signal to pass through the latch element (225) (figure 4, column 5 lines 30-32 and column 6 lines 48-62).

It would have been obvious to one skilled in the art at the time the invention was made to use Nataraj's match latch circuit (203) having the plurality of AND gates (223) and plurality of latch elements (225) such that each latch element (225) is enabled to pass/output a match signal [generated by a AND gate (223)] to Ichiriu's priority encoder (114) and Ichiriu's FLAG circuit (112). One having ordinary skill in the art would be motivated to combine the teachings of Ichiriu and Nataraj because the combination of Ichiriu's priority encoder [114] & FLAG circuit [112] and Nataraj's priority encoder/flag logic circuit (215) comprises inputs of match signals and outputs of match addresses and match flag (Ichiriu: figure 1, column 3 line 64-column 4 line 13; Nataraj: figure 4, column 7 line 1-15).

Claim 10:

Ichiriu teaches that a comparand value is stored to the CAM array (101). Ichiriu also teaches that the results of any match between the comparand and a valid CAM word are outputted to a priority encoder (114) for outputting a CAM index (174), such a CAM index is an address of the CAM word corresponding to the selected match signal (column 4 lines 1-8).

Claims 12 and 14:

Ichiriu discloses the invention substantially as claimed. Ichiriu shows (figures 5 and 1) that a CAM array (101) includes a plurality of CAM cells (201) arranged in rows and columns, with each row of CAM cells (201) being coupled to a respective word line

and to a respectively match line (182). Each CAM (201) includes a compare circuit to compare the content of the memory cell with a comparand signal (figure 5, column 6 line 33-column 7 line 13).

Ichiriu does not explicitly teach a circuit for determining a status of the match line under tested based on result of a search operation and a signal on the match line after confirming proper operation of a control line used to generate a signal.

Nataraj, however, teaches (figure 4) that a match latch circuit (203), which is connected to precharge circuits (233) and match lines (241), comprises latching circuits (221), each latching circuit comprises an AND gate (223) and a latch element (225). Each AND gate (223) has a first input coupled to receive a detect signal (224) and a second input coupled to a corresponding one of the match lines (241). The AND logic gate (223) outputs a logic-level match signal in high or low state according to whether the signal level of the corresponding match line is above or below a threshold. The latch signal (226) is supplied to a latch enable input of the latch element (225) enables the logic-level match signal to pass through the latch element (225) (figure 4, column 5 lines 30-32 and column 6 lines 48-62).

It would have been obvious to one skilled in the art at the time the invention was made to use the combination of Nataraj's precharge circuits (233) and Nataraj's match latch circuit (203) having the plurality of AND gates (223) and plurality of latch elements (225) such that each latch element (225) is enabled to pass/output a match signal [generated by a AND gate (223)] to Ichiriu's priority encoder (114) and Ichiriu's FLAG circuit (112). One having ordinary skill in the art would be motivated to combine the

teachings of Ichiriu and Nataraj because the combination of Ichiriu's priority encoder [114] & FLAG circuit [112] and Nataraj's priority encoder/flag logic circuit (215) comprises inputs of match signals and outputs of match addresses and match flag (Ichiriu: figure 1, column 3 line 64-column 4 line 13; Nataraj: figure 4, column 7 line 1-15).

Claim 13:

Ichiriu also teaches a priority encoder (114), in responsive to the results of any match between the comparand and a valid CAM word, for outputting a CAM index (174), such a CAM index is an address of the CAM word corresponding to the selected match signal (column 4 lines 1-8).

Claim 17:

Ichiriu discloses the invention substantially as claimed. Ichiriu shows (figure 5) that a CAM array (101) includes a plurality of CAM cells (201) arranged in rows and columns, with each row of CAM cells (201) being coupled to a respective word line. Each CAM (201) includes a compare circuit to compare the content of the memory cell with a comparand signal. Each of the match lines (182) is precharged to a high logical level at the start of a comparison operation, but pulled down to a low logical level by the compare circuit within any attached CAM cell (201) that receives comparand signal which do not match the stored data value. In this configuration, any match line (182) not pulled low constitutes a match signal (figure 5, column 6 lines 33-column 7 line 13).

Ichiriu does not explicitly teach the enabling circuitry for enabling a match line after confirming proper operation of a control line.

Nataraj, however teaches (figure 4) that a match latch circuit (203), which is connected to the precharge circuits (233) and match lines (241), comprises latching circuits (221); each latching circuit (221) comprises an AND gate (223) and a latch element (225). Each AND gate (223) has a first input coupled to receive a detect signal (224) and a second input coupled to a corresponding one of the match lines (241). Each of latch elements (225), in response to a latch signal, enables the corresponding logic-level match signal to pass through the latch element (225) after a corresponding AND gate (223), in responsive to a detect signal, outputs a logic-level match signal in high or low state according to whether the signal level of the corresponding match line is above or below a threshold (figure 4, column 5 lines 30-32 and column 6 lines 48-62).

It would have been obvious to one skilled in the art at the time the invention was made to use the combination of Nataraj's precharge circuits (233) and Nataraj's match latch circuit (203) having a plurality of AND gates (223) and a plurality of latch elements (225) such that each latch element (225) is enabled to pass/output a match signal [generated by a AND gate (223)] to Ichiriu's priority encoder (114) and Ichiriu's FLAG circuit (112). One having ordinary skill in the art would be motivated to combine the teachings of Ichiriu and Nataraj because the combination of Ichiriu's priority encoder (114) & FLAG circuit (112), and Nataraj's priority encoder/flag logic circuit (215) comprises inputs of match signals and outputs of match addresses and match flag

(Ichiriu: figure 1, column 3 lines 64-column 4 line 13; Nataraj: figure 4, column 7 line 1-15).

Claim 19:

Ichiriu teaches that each row of CAM cells (201) is coupled to a respective word line (181) and to a respective match line (182) (figure 5, column 6 lines 35-37).

Claims 20-21:

These claims are similar to claims 17 and 19 with additional recited control circuitry for resetting the enabling circuitry. Ichiriu teaches that the CAM array (101) includes circuitry to force validity value with each validity storage cell (202) to a reset state to prevent assertion of a match signal by pulling the match line low for the corresponding row of CAM cells (column 7 lines 49-65, column 8 lines 20-24).

Claim 22:

Ichiriu teaches that a comparand value is stored to the CAM array (101). Ichiriu also teaches that the results of any match between the comparand and a valid CAM word are outputted to a priority encoder (114) for outputting a CAM index (174), such a CAM index is an address of the CAM word corresponding to the selected match signal (column 4 lines 1-8).

Claim 23:

This claim is similar to claim 12 except the additional recited processor and the additional recited circuit for determining a status of a write enable signal to generate a signal on the word lines.

Ichiriu teaches that a system (960) includes a CAM device (961), a CPU (962) and a network processing unit (NPU) (963) (figure 38, column 37 lines 26-45). Ichiriu also teaches an address circuit (103) includes an address selector (125) that responds to the select signal (118) by selecting an address (178) so that an address decoder (127) decodes the selected address (178) to activate one of a plurality of word lines (181) (figures 1 and 2, column 5 lines 17-27).

Claims 33-34:

Ichiriu discloses the invention substantially as claimed. Ichiriu shows (figure 5) that a CAM array (101) includes a plurality of CAM cells (201) arranged in rows and columns; with each row of CAM cells (201) being coupled to a respective word line. Each CAM (201) includes a compare circuit to compare the content of the memory cell with a comparand signal. Each of the match lines (182) is precharged to a high logical level at the start of a comparison operation, but pulled down to a low logical level by the compare circuit within any attached CAM cell (201) that receives comparand signal which do not match the stored data value. In this configuration, any match line (182) not pulled low constitutes a match signal (figure 5, column 6 lines 33-column 7 line 13).

Ichiriu teaches that the CAM array (101) includes circuitry to force validity value with each validity storage cell (202) to a reset state to prevent assertion of a match signal by pulling the match line low for the corresponding row of CAM cells (column 7 lines 49-65, column 8 lines 20-24).

Ichiriu does not explicitly teach the enabling circuitry for enabling a match line.

Nataraj, however teaches (figure 4) that a match latch circuit (203), which is connected to precharge circuits (233) and match lines (241), comprises latching circuits (221); each latching circuit (221), in responsive to a latch signal and a detect signal, outputs a logic-level match signal in high or low state according to whether the signal level of the corresponding match line is above or below a threshold (figure 4, column 5 lines 30-32 and column 6 lines 48-62).

It would have been obvious to one skilled in the art at the time the invention was made to use the combination of Nataraj's precharge circuits and Nataraj's match latch circuit (203) having a plurality of latching circuits (221), each of which to pass/output a match signal to Ichiriu's priority encoder (114) and Ichiriu's FLAG circuit (112). One having ordinary skill in the art would be motivated to combine the teachings of Ichiriu and Nataraj because the combination of Ichiriu's priority encoder (114) & FLAG circuit (112), and Nataraj's priority encoder/flag logic circuit (215) comprises inputs of match signals and outputs of match addresses and match flag (Ichiriu: figure 1, column 3 lines 64-column 4 line 13; Nataraj: figure 4, column 7 line 1-15).

Claim 35:

Ichiriu teaches that a comparand value is stored to the CAM array (101). Ichiriu also teaches that the results of any match between the comparand and a valid CAM word are outputted to a priority encoder (114) for outputting a CAM index (174), such a CAM index is an address of the CAM word corresponding to the selected match signal (column 4 lines 1-8).

Claim 39:

This claim is similar to claim 33 except that a router is being recited. Ichiriu teaches a routing device including a CAM device (961) (figure 38, column 37 lines 26-45).

Claims 40-41:

Claims 40-41 are rejected for reasons similar to those set forth against claims 34-35.

Claim 42:

This claim is similar to claims 1 and 12 with additional processing system having a processor. Ichiriu shows a system (960) including a CAM device (961), a CPU (962) and a network processing unit (NPU) (963) (figure 38, column 37 lines 26-45).

Response to Arguments

4. Applicant's arguments filed October 16, 2007 have been fully considered but they are not persuasive.

The provionsional rejections on the ground of non-statutory obviousness-type double patenting (for claims 1-8, 10, 13, 19 and 42) have been withdrawn due to the terminal disclaimer being filed on October 16, 2007.

Claims 1-7:

(a) The applicant argues that there is no reason to combine Ichiriu and Nataraj. The examiner, however, respectfully traverses the applicant's remark.

Both Ichiriu (figure 1) and Nataraj (figure 4) teaches CAM having match lines providing outputs to the PE and the flag logic. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to use Nataraj's match latch circuit (203) having the plurality of AND gates (223) and plurality of latch elements (225) such that each latch element (225) is enabled to pass/output a match signal [generated by a AND gate (223)] to Ichiriu's priority encoder (114) and Ichiriu's FLAG circuit (112). One having ordinary skill in the art would be motivated to combine the teachings of Ichiriu and Nataraj because the combination of Ichiriu's priority encoder [114] & FLAG circuit [112] and Nataraj's priority encoder/flag logic circuit (215) comprises inputs of match signals and outputs of match addresses and match flag (Ichiriu: figure 1, column 3 line 64-column 4 line 13; Nataraj: figure 4, column 7 line 1-15).

(b) The applicant states that neither Ichiriu nor Nataraj teaches the feature of resetting all match lines of the memory device. Applicant also states that claim 1 recites resetting all match lines which, in one disclosed embodiment (in the specification), means that the TM _ML RESET signal pulses which sends a low signal to an AND gate, thus disabling the AND gate.

The examiner, however, disagrees against the applicant's remarks.

Firstly, base on the limitation of claim, there is no specific limitation recited on how the resetting is being done on the match lines. So Ichiriu's precharging the match lines to a high logical level (figure 5, column 6 lines 61-66) would have been similar to the recited feature of resetting the match lines (in claim 1).

Secondly, applicant's remarks of resetting all match lines means disabling an AND gate in responsive to a low signal from the TM_ML RESET signal pulses. However, such an AND gate and TM_ML RESET signal pulses do not have any patentable weight because these elements are not recited in claim 1.

(c) The applicant also argues that none of the references teaches confirming proper operation of a control line used to enable output from a match line under test.

Examiner, however, disagrees applicant's remarks. Ichiriu states that at the start of a comparison operation, each of the match lines (182) is precharged to a high logical level (column 6 lines 61-column 7 lines 4). In addition, Nataraj also teaches (figure 4) that within the match latch circuit (203) having a plurality of latching circuits, each latching circuit has a AND gate (223) and a latch element (225). Such a plurality of

AND gates (223) and such a plurality of latch elements (225) are connected match lines (241) to used for passing/confirming the match lines (241).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to use Nataraj's match latch circuit (203) having the plurality of Nataraj's AND gates (223) and plurality of Nataraj's latch elements (225) such that the combination of each AND gate (223) and each latch element (225) is enabled to pass/confirm/output a match signal (as suggested by Nataraj) to Ichiriu's priority encoder (114) and Ichiriu's FLAG circuit (112). One having ordinary skill in the art would be motivated to combine the teachings of Ichiriu and Nataraj because the combination of Ichiriu's priority encoder [114] & FLAG circuit [112] and Nataraj's priority encoder/flag logic circuit (215) comprises inputs of match signals and outputs of match addresses and match flag (Ichiriu: figure 1, column 3 line 64-column 4 line 13; Nataraj: figure 4, column 7 line 1-15).

(d) Applicant further argues that none of the references teaches "comparing said result of said search operation with an expected result of said search operation, said expected result comprising an expected match indication on the match line under test; confirming proper operation of said memory device if said result of said search operation is equal to said expected result of said search operation; and indicating an error of said memory device if said result of said search operation is not equal to said expected result of said search operation".

Examiner respectfully traverses applicant's position. Such limitations are taught by Ichiriu.

As being rejected in the 103 rejection in paragraph 3 above, Ichiriu shows (figure 1) that a CAM array (101) includes a plurality of CAM cell arranged in rows for storing CAM words. Each CAM cell (201) includes a compare circuit to compare the content of the memory cell with a comparand signal. A comparand register (115) is used to store a comparand value received via the comparand bus (143) and outputs the comparand value to the CAM array (101). During a compare operation, the comparand may be masked by a global mask value, and then compared simultaneously with all the CAM words stored in the CAM array. Each of the rows of CAM cell is coupled to a corresponding match line (182) and any match between the comparand and a valid CAM word results in a match signal being output to the flag circuit (112). The flag circuit (112) then outputs a match flag signal to indicate that a match has occurred (figure 1, column 3 line 29 - column 4 line 34, column 6 lines 42-47).

Claims 8-10:

(e) The applicant alleges that rejection of claim 8 in the office action is deficient for the same reasons set forth in claim 1 above. Well, since claims 1-7 are still rejected and are rebutted as stated above, then claims 8-10 are also rejected and rebutted as stated in paragraphs 3 and 4(a)-(d) above.

Claims 12-14:

(f) For claim 12, the applicant again alleges that neither Ichiriu nor Nataraj teach nor suggest a circuit coupled to a match line under test, a word line, and a test mode match line reset signal and the circuit for determining a status of the match line under test based on a result of a search operation and a signal on the match line under test after confirming proper operation of a control line used to generate a signal on the word line.

The examiner, however, respectfully traverses applicant's remarks.

Ichiriu does not explicitly teach a circuit for determining a status of the match line under tested based on result of a search operation and a signal on the match line after confirming proper operation of a control line used to generate a signal. Nataraj, however, teaches (figure 4) that a match latch circuit (203), which is connected to precharge circuits (233) and match lines (241), comprises latching circuits (221), each latching circuit comprises an AND gate (223) and a latch element (225). Each AND gate (223) has a first input coupled to receive a detect signal (224) and a second input coupled to a corresponding one of the match lines (241). The AND logic gate (223) outputs a logic-level match signal in high or low state according to whether the signal level of the corresponding match line is above or below a threshold. The latch signal (226) is supplied to a latch enable input of the latch element (225) enables the logic-level match signal to pass through the latch element (225) (figure 4, column 48-62).

It would have been obvious to one skilled in the art at the time the invention was made to use the combination of Nataraj's precharge circuit (233) and Nataraj's match

latch circuit (203) having the plurality of AND gates (223) and plurality of latch elements (225) such that each latch element (225) is enabled to pass/output a match signal [generated by a AND gate (223)] to Ichiriu's priority encoder (114) and Ichiriu's FLAG circuit (112). One having ordinary skill in the art would be motivated to combine the teachings of Ichiriu and Nataraj because the combination of Ichiriu's priority encoder [114] & FLAG circuit [112] and Nataraj's priority encoder/flag logic circuit (215) comprises inputs of match signals and outputs of match addresses and match flag (Ichiriu: figure 1, column 3 line 64-column 4 line 13; Nataraj: figure 4, column 7 line 1-15).

(g) the applicant further alleges that neither Ichiriu nor Nataraj teach nor suggest a test mode match line reset signal because neither Ichiriu nor Nataraj teach a signal that resets all match lines.

Both Ichiriu and Nataraj do teach the test mode match line reset signal. Nataraj does teach that each match line (241) being precharged between successive compare operations by a respective precharge circuit (233) (figure 4, column 5 lines 30-32). In addition, Ichiriu does teach that during a compare operation, each of the match lines (182) is precharged to a high logical level at the start of a comparison operation (figure 5, column 6 lines 61-66).

(h) The applicant argues that neither Ichiriu nor Nataraj teach nor suggest confirming proper operation of a control line used to generate a signal on the word line.

However, such limitations are not recited. What is being recited is only the condition of "**after** confirming proper operation of a control line used to generate a signal on the word line". In other words, base on an apparatus claim in claim 12, no specific device/element is recited with the function of confirming proper operation of a control line.

Claims 17, 19 and 20-22:

(i) The applicant also argues that rejection of claims 17, 19 and 20-22 in the office action is deficient for the same reasons set forth in claim 1 above. Well, since claims 1-7 are still rejected and rebutted as stated above, then claims 17, 19 and 20-22 are also rejected and rebutted as stated in paragraphs 3 and 4(a)-(d) above.

Claim 23:

(j) The applicant further argues that rejection of claim 23 in the office action is deficient for the same reasons set forth in claim 12 above. Well, since claim 12 is still rejected and rebutted as stated above, then claim 23 is also rejected and rebutted as stated in paragraphs 3 and 4(f)-(g) above.

Claims 33-35 and 39-41:

(k) The applicant states that neither Ichiriu nor Nataraj teach nor suggest resetting all match lines.

Examiner, however, does not agree applicant's statement. In fact, both Ichiriu and Nataraj do teach the feature of resetting all match lines. Nataraj does teach that each match line (241) being precharged between successive compare operations by a respective precharge circuit (233) (figure 4, column 5 lines 30-32). In addition, Ichiriu does teach that during a compare operation, each of the match lines (182) is precharged to a high logical level at the start of a comparison operation (figure 5, column 65 lines 61-66).

(l) The applicant also states claims 40-41 depend on from 39 and therefore rejections of claims 40-41 should be withdrawn.

The examiner, however, respectfully traverses applicant's remark. Base on claims 40 and 41, these claims are improperly depending on a cancelled claim (which is claim 36) (see 112/2nd rejection in paragraph 2 above). Therefore, rejections for these claims still stand as stated in the 103 rejection (in paragraph 3 above).

Claim 42:

(m) The applicant alleges that neither Ichiriu nor Nataraj teach nor suggest the feature of resetting all match lines and the feature of confirming proper operation of a control line used to enable output from a match line under test.

The examiner does not agree applicant's position. In fact, both features are taught by Ichiriu and Nataraj as described in paragraphs 3 and 4(b), 4(c) and 4(g) above.

5. This is a Request for Continuation Examination of applicant's earlier Application No. 10/648,311. All claims are drawn to the same invention claimed in the earlier application and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the earlier application. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action in this case. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no, however, event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. Tu whose telephone number is (571) 272-3831. The examiner can normally be reached on Mon-Thur. 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Christine T. Tu
Primary Examiner
Art Unit 2117

January 5, 2008